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Information Disclosure Statement by Applicant (Use several sheets if necessary)	Applicant: Xinli Gu et al.	
	Filed: January 4, 2002 Group: ~~2858~~ 2825	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	A	5,912,901	6/15/1999	Adams et al.	371	22.5	3/24/1997

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Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	B	Gu et al., "A Fast Timing Closure Technique for Industrial Use of Logic BIST", May 2001, pp. 1-10.
	C	Hetherington et al., "Logic BIST for Large Industrial Designs: Real Issues and Case Studies", ITC International Test Conference, 1999, pp. 358-367.
	D	Nakao et al., "Low Overhead Test Point Insertion for Scan-Based BIST", 1999, pp. 348-357.
	E	Cheng et al., "Timing-Driven Test Point Insertion for Full-Scan and Partial-Scan BIST", 1995, pp. 506-514.

Examiner	Date Considered 9 - DECEMBER - 2004

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.